Atty. Dkt. No. 039153-0298 (F0785)

REMARKS

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and in view of the reasons which follow.

Claims 1-24 stand rejected. Claims 9, 13, 14 and 19 have been amended. No new matter is added in the amendments to the claims. Claims 9, 13, 14 and 19 have been amended in a non-limiting fashion to more clearly recite the invention and to correct typographical errors. Accordingly, Claims 1-24 remain pending in the application.

In paragraph 2 of the Office Action, the Examiner has objected to the disclosure. Applicants have provided the requested information and the amended specification in accordance with the Examiner's suggestion. No new matter is added. Accordingly, withdrawal of the objection of the specification is respectfully requested.

In paragraphs 3-4 of the Office Action, claims 1, 9, 16 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 9, 16 of co-pending Application No. 09/819,342 in view of US Pat. 5,876,903 (Ng). The Examiner states:

> The instant invention discloses a method of trimming a resist pattern by modifying the patterned resist feature in an ion dominated environment.
>
> The instant claims disclose: modifying the top of the resist pattern in an ion dominated environment that renders the modified portion of the patterned feature more resistant to an etching operation than the lower portion; and using the difference in the etch rates to trim (the lateral dimensions of) the feature. Application to the fabrication of an integrated circuit with sub-lithographic dimensioned features is disclosed.
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> The '342 application is directed towards a method of trimming a feature patterned on a photoresist after modifying the patterned resist feature with electron irradiation.
>
> The cited reference claims : modifying the top of the resist pattern, that renders the top portion of the patterned

> feature more resistant to an etching operation than the lower portion; and using the difference in the etch rates to trim (the lateral dimensions of) the feature. The technique is used to fabricate integrated circuits with sub-lithographic dimensioned features.
>
> The '342 reference does not teach the use of ion beams to harden the resist features.
>
> Ng teaches that the surface layer of a patterned resist feature may be hardened by ion bombardment,, which results in a virtual hard mask (2;28-36). The ion beam is directed towards the top as well as the sidewalls to harden all the exposed surfaces equally and create a uniform hardened layer (4;39-61). this reduces the etching rate of the sides more than the top which is the intended goal of the invention (4;62-5;19). However selective hardening of the top of the feature by a directed beam is known in the art.

Applicants respectfully traverse the rejection. However, to advance prosecution, Applicants have provided a terminal disclaimer attached hereto. Accordingly, withdrawal of the obviousness-type double patenting rejection is respectfully requested.

In paragraphs 5 and 6 of the Office Action, Claims 9-15 and 19 are rejected under 35 USC § 112, second paragraph. The Examiner states:

> Claims 9, 13 and 14 recite the limitation "the ashing step" in lines 13, 23 and 26 respectively. There is insufficient antecedent basis for this limitation in the claim.
>
> While resist trimming may be performed by ashing this is not defined in any of the steps and makes the claims vague and indefinite. This rejection may be overcome by rephrasing claim 9 to recite "*an* ashing step" in line 13. Claims 10-12 and 15 depend directly or indirectly from claim 9.
>
> Claim 19 recites the limitation that "top portion has a negligible etch rate". The term "negligible" is a relative term not well defined and makes the claim vague and indefinite. The specification discloses etch rates that are 15% - 70% slower than untreated resist as being negligible (p.10; #0036) and another measure suggests 10% - 50% loss of vertical height (p.13;#0044) as being negligible.

Applicants have amended Claims 9, 13, 14 and 19 in accordance with the Examiner's suggestions. Accordingly, withdrawal of the rejection of claims 9, 13, 14 and 19 is respectfully requested.

In paragraph 7 of the Office Action, Claims 1-24 are rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,982,195 (Yen) in view of U.S. Patent No. 6,200,903 (Oh) and U.S. Patent No. 4,394,211 (Uchiyama). The Examiner states:

> Yen teaches a method of trimming a resist pattern to form a trimmed gate on an FET. Control of line widths is critical to the process. A resist layer (22) is formed on an (ARC) anti-reflective coating (20) formed over a gate stack (Fig. 1). The resist is patterned with a width W1 larger than the intended gate width. The resist feature is plasma hardened (Fig.3) by a "plasma pretreatment" (9;10-10;5). The pre-treatment exposes the resist to a flood of ions comprising Ar+ and F+ ions. The hardened resist pattern and the ARC are plasma etched. The lateral etch rate is greater than the vertical etch rate (10;6-35); as a result the pattern width is reduced to W2 (Fig. 4). This pattern is transferred to the gate layer by anisotropic etching to preserve the reduced gate width and pattern height integrity (Figs. 5-6). The resist and ARC are removed (Fig.7). Yen patterns features with near UV (365nm) radiation to form sub-lithographic dimensioned gates. Etch bias of 145 nm is reported (16;5-14)
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> Yen does not teach modifying the trim rate with the dose of the ions (cl.4) or the energy and mass of the ions (cl.5,15). It does not teach implanting Ar+, F+ or Kr+ ions (cl.17,20,21). Yen does not teach patterning 150 nm features using deep UV radiation or removing the top of the resist before etching the substrate (cl.22-23).
>
> Oh teaches Ar+ implantation into patterned resist features to reduce the etch rate. The resist pattern is formed on a substrate to e etched (Fig.5) The patterned features are irradiated with Ar+ ions (Fig.6). The implantation parameters include the angle, dose and depth (3;24-53). Oh teaches that the resist is significantly etched in the vertical dimension (cl.22) during transfer of pattern to the substrate (Fig. 7 & 4;1-17).

> Oh does not teach modifying the etch rate with the dose. It does not teach patterning 150 nm features using deep UV radiation.
>
> Uchiyama teaches hardening a polyimide resin layer by ion bombardment to minimize etchant attack. The etch rate is dependent on the dosage (Fig. 1). The etch rate may be varied by the mass and energy of the ion (3;10-18). It is well known in the art to adjust the depth by controlling the energy of the ion.

Applicants respectfully traverse the rejection. Yen, Oh, and Uchiyama are referred to below as the cited art.

Each of the independent claims recites a method in which a patterned photoresist feature is treated to have a modified top portion and then trimmed to a sub-lithographic dimension. The trimming step involves different etching rates due to the modified top portion. Claim 1 recites:

> modifying the top portion of the feature . . . and trimming the feature to form a trimmed feature, wherein a vertical trim rate and a lateral trim rate are associated with the feature and the vertical trim rate is slower than the lateral trim rate due to the modified top portion . . . .

Claim 9 recites:

> modifying the patterned photoresist layer to form a top portion . . ., the top portion having a top etch rate and the bottom portion having a bottom etch rate, wherein the top etch rate is different from the bottom etch rate; and
>
> trimming the patterned photoresist layer to change the at least one feature to have a sub-lithographic lateral dimension . . . .

Claim 16 recites:

> changing at least a portion of the photoresist layer, wherein a top portion of the feature patterned on the photoresist layer is changed to have a different etch rate from a bottom portion of the feature patterned on the photoresist layer;
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> trimming the feature patterned on the photoresist layer to a sub-lithographic dimension.

Therefore, each of Claims 1, 9 and 16 recites an advantageous process where a top portion is modified so that the photoresist feature has a vertical etch rate different than the lateral etch rate. An embodiment of these process steps are described with reference to FIGURES 4 and 5 from page 10 to page 13 of the present patent application.

Such a feature is not shown, described or suggested in the cited art. The Examiner relies on Yen to teach a trim etching step in which the lateral etch rate is greater than the vertical etch rate. However, the portion of Yen cited by the Examiner does not show, describe or suggest such a feature. Yen does not mention different lateral and vertical etch rates. Indeed, from the figures of Yen, it appears as though the vertical etch rate is greater than the lateral etch rate. Indeed, Yen relies on a two layer photoresist structure in which the blanket focusing layer has a greater lateral etch rate than the photoresist feature. Yen even discusses that a photoresist feature may be undercut due to this increased lateral etching, thereby indicating that Yen desires a small lateral etching rate for the photoresist feature Therefore, Yen cannot provide a suggestion for the differing etch rates due to the modified top portion.

Oh does not even mention trim etching. Indeed, Oh merely utilizes the lithographically patterned layer to etch an underlying layer. The treatment process is used to provide etch resistance during the etch step, not during a trim etching process. The etch step is for the underlying layer. See Oh, FIGURES 7 and 8. Indeed, Oh even discusses treatment at an angle to treat sides of the photoresist pattern. Therefore, Oh cannot provide the suggestion for the differing etch rates due to modification of the top portion.

Applicants respectfully submit that Uchiyama does not provide any suggestion for the treatment of the photoresist layer. Indeed, only one photoresist layer is mentioned for lithographic patterning in Uchiyama and that is layer 32. However, layer 32 is never trim etched or treated. Only polyimide layer 28 is treated. Applicants respectfully submit that the Examiner cannot take a polyimide layer in Uchiyama which is not utilized in any lithographic patterning step and then substitute that polyimide layer into a lithographic pattern step in Yen and Oh. This is especially true when Uchiyama does not provide any suggestions for treating its photoresist layer which is

at least two layers above the polyimide layer. Therefore, Uchiyama cannot provide a suggestion for the differing etching rates due to the modified top portion.

Further, Applicants submit that Oh and Yen teach away from the present invention. As discussed above, Oh teaches away from the present invention because it teaches the use of angled treatments. See Oh column 3, lines 31-39. Angled treatments would ensure that lateral sides are treated and different etching rates would not be achieved. Similarly, Yen teaches the use of a second layer, a blanket focusing layer, to achieve sub-lithographic dimensions Using two layers teaches away from the modification principle of the present invention. Indeed, Yen is completely ignorant of the advantages of modifying a single photoresist layer.

As discussed above, the cited art does not provide a suggestion for the features recited in Claims 1-20. In fact, Oh and Yen even teach away from the present invention. Accordingly, it is respectfully submitted that independent Claim 1 and its dependent Claims 2-8 and independent Claim 9 and its dependent Claims 10-15, and independent Claim 16 and its dependent Claims 17-20 are patentable over the cited art.

Applicants believe that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

Respectfully submitted,

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MARKED UP VERSION SHOWING CHANGES MADE

In the Specification:

[0001] The present application is related to U.S. Application No. [_____] 09/819,692 (Atty. Dkt. No. 39153/404) by Okoroanyanwu et al., entitled "Process for Preventing Deformation of Patterned Photoresist Features by Electron Beam Stabilization;" U.S. Application No. [_____] 09/820,143 (Atty. Dkt. No. 39153/405) by Okoroanyanwu et al., entitled "Improving SEM Inspection and Analysis of Patterned Photoresist Features;" U.S. Application No. [_____] 09/819,344 (Atty. Dkt. No. 39153/406) by Okoroanyanwu et al., entitled "Process for Reducing the Critical Dimensions of Integrated Circuit Device Features;" U.S. Application No. [_____] 09/819,342 (Atty. Dkt. No. 39153/403) by Shields et al., entitled "Process for Forming Sub-Lithographic Photoresist Features by Modification of the Photoresist Surface;" and U.S. Application No. [_____] 09/819,552 (Atty. Dkt. No. 39153/310) by Gabriel et al., entitled "Process for Improving the Etch Stability of Ultra-Thin Photoresist," all filed on an even date herewith and assigned to the Assignee of the present application.

In the Claims:

9. (Amended) An integrated circuit fabrication process, the process comprising:

developing a patterned photoresist layer, the patterned photoresist layer including at least one feature;

modifying the patterned photoresist layer to form a top portion and a bottom portion of the at least one feature, the top portion having a top etch rate and the bottom portion having a bottom etch rate, wherein the top etch rate is different from the bottom etch rate; and

trimming the patterned photoresist layer to change the at least one feature to have a sub-lithographic lateral dimension, whereby a sufficient vertical

thickness exists to maintain pattern integrity, wherein the modifying step is performed after the developing step and before the [ashing] trimming step.

13. (Amended) The process of claim 12, wherein a majority of the top portion and a laterally trimmed bottom portion comprises the at least one feature upon completion of the [ashing] modifying step, the laterally trimmed bottom portion having the sub-lithographic lateral dimension and the sufficient vertical thickness to maintain pattern integrity.

14. (Amended) The process of claim 13, further comprising removing the majority of the top portion after the [ashing] modifying step to form a trimmed feature.

19. (Amended) The process of claim 18, wherein the top portion has [a negligible] has an etch rate 15-70% slower than an untreated etch rate of the photoresist layer during the trimming step.